PATENT APPLICATION
Docket No. MS1-1536US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of		)
		)
	Gray	)
		)
Serial No.:	10/609,105	) Appeal No.
		)
Confirmation No.	9327	)
		)
Filed:	June 27, 2003	)
		)
For:	Cache Residency Test Instruction	)
		)
Examiner:	Thai, Tuan V.	)

The Honorable Commissioner of Patents
Mail Stop Appeal Brief - Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

BRIEF OF APPELLANT

The Applicant has filed a timely Notice of Appeal from the action of the Examiner in finally rejecting all of the claims that were considered in this application. This Brief is being filed under the provisions of 37 C.F.R. § 1.192. The Filing Fee, as set forth in 37 C.F.R. § 1.17(c), is submitted herewith.

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REAL PARTY IN INTEREST

The real party in interest is Microsoft Corporation, by way of assignment from Gray, who is the named inventive entity and is captioned in the present brief.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 11, 13-19, 21-23, 42-46, 48-50 and 56-67 are pending and are the subject of this appeal.

Claims 1-10, 12, 20, 24-41, 47, 51-55 and 68 are cancelled.

STATUS OF AMENDMENTS

None.

SUMMARY OF THE CLAIMED SUBJECT MATTER

A cache memory residency test instruction is described, which when executed by a processor unit, allows the processor unit to determine if a set of data resides in a cache memory and communicate a result of the determination to software being executed on the processor unit. The processor unit performs data processing of a processor chip, such as by performing instructions and the like. The cache memory stores data for use by the processor unit. The data may include instructions to be executed by the processor unit and data to be processed by the processor unit.

The residency instruction is issued by the processor unit in order to determine if a set of data resides in the cache memory. For example, the residency instruction may be used to query the cache memory to determine if the set of data is stored in the cache memory. As a result of the query, the processor unit may receive an indication as to whether the set of data is stored in the cache memory, which is then communicated to software being executed on the processor. By determining whether the set of data is stored in the cache memory, the software being executed on the processor unit may recognize characteristics that are likely to be encountered when accessing the set of data, such as a relative amount of time it will take to access the set of data, and the like.

Independent Claim 11 recites a method comprising:

- querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit (e.g., reference number 802, FIG. 8; paragraph [0069],

lines 3-9, page 25);

- receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory (e.g., reference number 804, FIG. 8; paragraph [0070], lines 10-13, page 25); and
- communicating the indication to an operating system being executed on the processor unit (e.g., reference number 806, FIG. 8; paragraph [0070], lines 14-15, page 25).

Independent Claim 19 recites a method comprising:

- comparing an address of a set data with at least one other address in a cache memory (e.g., reference number 906, FIG. 9; page 26, paragraph [0072], lines 3-9], wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;
- providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory (e.g., reference number 908, FIG. 9; page 26, paragraph [0073], lines 10-13), wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;
- establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included (e.g.,

reference numbers 502-508, FIG. 5; reference number 1016, FIG. 10; page 27, paragraph [0075], lines 13-20; page 28, paragraph [0078], lines 18-22); and

- communicating the indication, by the processor unit, to software being executed on the processor unit (e.g., reference number 1018, FIG. 10; page 27, page 28, paragraph [0078], lines 22-23).

Independent claim 42 recites for use on a processor unit (e.g., reference number 202, FIG. 2; page 11, paragraph [0032]) that is communicatively coupled to a comparison unit (e.g., reference number 216, FIG. 2) that is communicatively coupled to a cache memory (e.g., reference number 104, FIG. 2; page 11, paragraph [0033]), a cache residency test instruction, (e.g., reference number 102, FIG. 2; pages 10-11, paragraph [0031]) which when executed on the processor unit, configures the comparison unit to perform acts comprising:

- comparing an address received from the processor unit with an address in the cache memory (e.g., reference number 906, FIG. 9; page 26, paragraph [0072], lines 3-9];
- providing an indication to the processor unit based on the comparing of whether the address is included in the cache memory (e.g., reference number 908, FIG. 9; page 26, paragraph [0073], lines 10-13); and
- communicating the indication to an operating system being executed by the processor unit (e.g., reference number 806, FIG. 8; paragraph [0070], lines 14-15,

page 25).

Independent claim 45 recites a system comprising:

- a cache memory (e.g., reference number 104, FIG. 2; page 11, paragraph [0033]); and
- a processor unit (e.g., reference number 202, FIG. 2; page 11, paragraph [0032]) communicatively coupled to the cache memory, wherein the processor unit includes a cache residency test instruction (e.g., reference number 102, FIG. 2; pages 10-11, paragraph [0031]) that, when executed, configures the processor unit:
    - to query whether a set of data resides in the cache memory (e.g., reference number 802, FIG. 8; paragraph [0069], lines 3-9, page 25);
    - to receive an indication from the query of whether the set of data resides in the cache memory (e.g., reference number 804, FIG. 8; paragraph [0070], lines 10-13, page 25);
    - to establish a relative amount of time to access the set of data (e.g., reference numbers 502-508, FIG. 5; reference number 1016, FIG. 10; page 27, paragraph [0075], lines 13-20; page 28, paragraph [0078], lines 18-22); and
    - to communicate the indication and the relative amount of time to software being executed on the processor unit (e.g., reference number 806, FIG. 8; paragraph [0070], lines 14-15, page 25).

Independent claim 56 recites a processor chip comprising:

- a processor unit having a coupling for communicatively coupling the processor unit to a cache memory (e.g., reference number 202, FIG. 2; page 11, paragraph [0032]), wherein:
    - the processor unit includes storage for a cache residency test instruction (e.g., reference number 102, FIG. 2; pages 10-11, paragraph [0031]); and
    - an execution of the cache residency test instruction with the processor unit configures the processor unit to determine if a set of data resides in the cache memory (e.g., reference number 802, FIG. 8; paragraph [0069], lines 3-9, page 25; reference number 804, FIG. 8; paragraph [0070], lines 10-13, page 25), establish a relative amount of time to access the set of data (e.g., reference numbers 502-508, FIG. 5; reference number 1016, FIG. 10; page 27, paragraph [0075], lines 13-20; page 28, paragraph [0078], lines 18-22), and communicate a result of the determination and the relative amount of time to software being executed on the processor unit (e.g., reference number 806, FIG. 8; paragraph [0070], lines 14-15, page 25).

Independent claim 63 recites a computing device comprising:

a storage device (e.g., reference number 110, 112, FIG. 1; paragraphs [0026]-[0027], pages 8-9) ; and

a processor chip (e.g., reference number 106, FIG. 2; paragraph [0032], page 11, lines 10-13), communicatively coupled to the storage device, and including:

a cache memory (e.g., reference number 104, FIG. 2; paragraph [0033], page 11, lines 14-24); and

a processor unit (e.g., reference number 202, FIG. 2; paragraph [0032], page 11, lines 10-13); communicatively coupled to the cache memory, wherein the processor unit includes storage for a cache residency test instruction that, when executed by the processor unit, configures the processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to an operating system being executed on the processor chip.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 11, 13-17, 19, 21-22, 42-46, 48-50 and 56-67 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,560,676 to Nishimoto et al (hereinafter, "Nishimoto").

2. Claims 18 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimoto.

ARGUMENT

First Ground of Rejection Claims 11, 13-17, 19, 21-22, 42-46, 48-50 and 56-67 satisfy the requirements of 35 U.S.C. § 102(e) and therefore are not anticipated by Nishimoto.

(A). Nishimoto does not Disclose an Operating System

Claim 11 recites a method comprising:

- querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit;
- receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory; and
- communicating the indication to an operating system being executed on the processor unit.

Nishimoto does not disclose these features.

The Examiner, in rejecting claim 11, asserts ""communicating the indication to an operating system being executed on the processor is equivalently taught as the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the operating system within the processor (e.g., see column 5, lines 62-65)." *See Office Action Dated January 17, 2006, Page 7.* The asserted portion is excerpted as follows for the sake of convenience:

> Using the select signal 118, the selector 108 selects a piece of data and a tag from 4 pieces of data and 4 tags read at the same

> time, and outputs read data 114 and a read tag 115 as a result of the load instruction. *See Nishimoto, Col. 5, Lines 65-65.*

In neither the above referenced portion, nor elsewhere in Nishimoto, is "communicating the indication to an operating system being executed on the processor unit" as recited in Claim 11 disclosed. Indeed, the words "operating system" are not even included within the text of Nishimoto.

As is well settled, anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). In the present case, the Examiner seems to be applying an "equivalence" standard, the support for which is unclear to the Applicant and is respectfully submitted to be in error.

The Applicant respectfully requested that the Examiner state with specificity as to which element of Nishimoto is being asserted as the "operating system" of Claim 11. To date, the Examiner has not done so. Thus, it is respectfully submitted that the Examiner has not met the burden in making the rejection, "[w]here a major technical rejection is proper, it should be stated with a full development of reasons rather than by a mere conclusion coupled with some stereotyped expression." *M.P.E.P. §707.07(g)* Regardless, because each element of Claim 11 (e.g., an operating system) is not included in Nishimoto, it is respectfully submitted that a *prima facie*

case of anticipation has not been established and therefore the Applicant respectfully requests that the Board overturn the rejection.

Claims 42 and **63** are also independent claims and are allowable based on the reasons recited above. As previously described, Nishimoto does not even include the words "operating system". Therefore, Nishimoto cannot disclose "communicating the indication to ***an operating system*** being executed on the processor unit" as recited in Claim 42 nor "communicate a result of the determination to ***an operating system*** being executed on the processor chip" as recited in claim 63. Accordingly, the Applicant respectfully requests that the Board overturn the rejection.

Claims 13-18 depend either directly or indirectly from Claim 11 and are allowable as depending from an allowable base claim. **Claims 43-44** depend either directly or indirectly from Claim 42 and are allowable as depending from an allowable base claim. **Claims 64-67** depend either directly or indirectly from Claim 63 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in their respective independent claims, are neither shown nor suggested in the references of record, either singly or in combination with one another. Accordingly, the Applicant respectfully requests that the Board overturn the rejection.

(B). Nishimoto does not Disclose Communication of an Indication to Software of Which Level of a Plurality of Levels in a Cache Memory contains an Address of a Set of Data

Claim 19 recites a method comprising:

- comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;
- providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;
- establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included; and
- communicating the indication, by the processor unit, to software being executed on the processor unit.

Nishimoto does not disclose these features.

Beginning at page 10 of the subject Application, exemplary execution of a residency instruction is described. An execution of the residency instruction is used to improve the interaction of processor chip with the cache memory, and more particularly, to improve performance of software being executed on the processor

chip. The residency instruction, when executed on the processor chip, is used to determine if a set of data resides in the cache memory. Through execution of the residency instruction, the processor chip may recognize characteristics likely to be encountered when accessing the set of data. For example, characteristics of data access may include whether the set of data resides in the cache memory, and therefore may be accessed with minimal delay, or whether the set of data resides in other portions of the memory, such as RAM, peripheral memory, and the like. Therefore, the processor chip may establish a relative amount of time it will take to access the set of data, without actually accessing the set of data, e.g., reading or writing the set of data. The processor chip may communicate a result of the determination to software being executed on the processor chip such that the software may use the result to plan the next actions to be performed when executing the software. For instance, the software may determine which operation to perform first based on whether a set of data that will be the subject of the operation is available from the cache memory.

In some instances, a cache memory may include a plurality of levels. For instance, beginning at page 12 of the subject Application, each of the levels of the cache memory may be configured to provide different functionality when used in conjunction with the processor unit. For example, the level one cache memory may provide access to data stored in the level one cache memory at a rate which is equal to or close to the processor unit's speed, e.g. an amount of time taken to execute an

instruction by the processor unit. The level two cache memory may be configured to store a greater amount of data than the amount of data stored in the level one cache memory. The level two cache memory, however, may provide access to data at a slower rate than the level one cache memory. *See subject Application, Page 12 and FIG. 2.*

The Examiner, in the rejection of Claim 19, asserts FIGS. 3 and 4 of Nishimoto and column 4, lines 31 et seq. as disclosing a cache memory having a plurality of levels, the portions of which are excerpted as follows for the sake of convenience:

> FIG. 3 is a schematic block diagram of cache memory system 100. According to this embodiment, the cache memory system has a cache size of 128K bytes and a block size of 128 bytes, and employs a 4-way set associative system. The cache memory system uses LRU as a block replacement algorithm, and is controlled by a store through method. TI should be noted that in the figure, portions of the load/store unit 18 not related to the present invention are not shown. *See Nishimoto, Col. 4, lines 40-48.*

However, neither the above excerpted portion, the asserted figures nor elsewhere in Nishimoto is a cache memory having different levels disclosed. Rather, the above referenced portion clearly describes a single-level cache memory. Accordingly, since each claimed element (e.g., cache memory having a plurality of levels) is not disclosed in Nishimoto, it is respectfully submitted that a *prima facie* case of anticipation has not been established and the Applicant respectfully requests that the Board overturn the rejection.

Claims 21-23 depend either directly or indirectly from Claim 19 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in their respective independent claim, are neither shown nor suggested in the references of record, either singly or in combination with one another. Accordingly, the Applicant respectfully requests that the Board overturn the rejection.

(C). Nishimoto does not Disclose Communication of an Indication of a Relative Amount of Time to Software Being Executed on a Processor Unit and further the "Most Probably" Standard used by the Examiner is not Supported by 35 U.S.C. §102(e)

Claim 45 recites a system comprising:

- a cache memory; and
- a processor unit communicatively coupled to the cache memory, wherein the processor unit includes a cache residency test instruction that, when executed, configures the processor unit:
    - to query whether a set of data resides in the cache memory;
    - to receive an indication from the query of whether the set of data resides in the cache memory;
    - to establish a relative amount of time to access the set of data; and
    - to communicate the indication and the relative amount of time to software being executed on the processor unit.

Nishimoto does not disclose these features.

The Examiner first asserts that "the indication to software being executed on the processor unit is taught as when the data resides the cache (cache hit), a '1' is outputted as a hit signal 116". *See Office Action Dated January 17, 2006, Page 15.* The Examiner then asserts that "when a central processing unit is referring to data and instructions from a particular space within physical memory, it will most probably, once again, refer to the data and instructions from that space (temporal locality; e.g. see column 2, lines 20 et seq.) wherein the process have to establish amount of time to access said set of data; and the hit data (read data 114 and read tag 115) are outputted to the requested processor known to the software within the processor (e.g. see column 5, lines 62-65)". *See Office Action Dated January 17, 2006, Page 16.* First of all, it is respectfully submitted that a standard of "it will most probably" asserted by the Examiner is clearly not within the standard of anticipation nor even obviousness. As previously described, anticipation requires the disclosure in a single prior art reference of each element of the claim under consideration, not that the reference "will most probably" include the element. The Applicant respectfully requested that the Examiner further explain with specificity as to how the asserted portions disclose the claimed features, but to date the Examiner has not done so.

Regardless, the Applicant respectfully submits that the above recited features are not disclosed by Nishimoto. The only mention of read data and read tag in Nishimoto is described as follows:

> The select way control circuit 113 determines the way to be read according to a determination result by the hit/miss determination circuit 122. When the determination result is a cache hit (the hit signal 116 is "1"), the select way control circuit 113 outputs the way number indicated by the hit way signal 119, as a select way signal 117. This select way signal 117 is also used as a select signal 118 to the selector 108. Using the select signal 118, the selector 108 selects a piece of data and a tag from 4 pieces of data and 4 tags read at the same time, and outputs read data 114 and a read tag 115 as a result of execution of the load instruction. *See Nishimoto, Col. 5, Lines 55-65.*

As shown in the above excerpted portion, however, neither the read data nor the read tag "communicate **the indication and the relative amount of time** to software being executed on the processor unit" as recited in Claim 45.

Accordingly, since each claimed element is not disclosed in Nishimoto, it is respectfully submitted that a *prima facie* case of anticipation has not been established and therefore the Applicant respectfully requests that the Board overturn the rejection.

Claim 56 is also an independent claim and is allowable based on the reasons recited above. As previously described, Nishimoto does not communicate the indication and the relative amount of time. Accordingly, the Applicant respectfully requests that the Board overturn the rejection..

Claims 46, 48-50 depend either directly or indirectly from Claim 45 and are allowable as depending from an allowable base claim. **Claims 57-62** depend either directly or indirectly from Claim 56 and is allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in their respective independent claim, are neither shown nor suggested in the references of record, either singly or in combination with

one another. Accordingly, the Applicant respectfully requests that the Board overturn the rejection.

Second Ground of Rejection Claims 18 and 23 satisfy the requirements of 35 U.S.C. § 103(a) and are thus patentable over Nishimoto for at least the reasons recited in relation to the first ground of rejection. Additionally, Nishimoto does not teach or suggest a computer-readable medium having instructions as recited in these claims, and therefore the Applicant respectfully requests that the Board overturn this rejection.

CONCLUSION

The Applicant respectfully considers this application to be in condition for allowance and respectfully requests the Board to overturn the final rejection and that the Examiner pass this application to allowance.

Dated this 14th day of August, 2006.

Respectfully submitted,

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APPENDIX: CLAIMS ON APPEAL

Claims 1-10 (cancelled).

11. (previously presented): A method comprising:

querying whether a set of data resides in a cache memory that is communicatively coupled to a processor unit;

receiving an indication at the processor unit from the querying which indicates whether the set of data resides in the cache memory; and

communicating the indication to an operating system being executed on the processor unit.

12. (cancelled).

13. (original): A method as described in claim 11, further comprising establishing a relative amount of time to access the set of data by the processor unit based on the indication which indicates whether the set of data resides in the cache memory.

14. (original): A method as described in claim 11, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

15. (original): A method as described in claim 11, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

16. (original): A method as described in claim 11, wherein the querying and the receiving are performed without reading the set of data from the cache memory to the processor unit and without writing the set of data from the processor unit to the cache memory.

17. (original): A method as described in claim 11, further comprising:

comparing an address of the set data with at least one other address in the cache memory, wherein the cache memory includes a plurality of levels; and

providing, based on the comparing, an indication to the processor unit of whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included.

18. (original): One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 11.

19. (previously presented): A method comprising:

comparing an address of a set data with at least one other address in a cache memory, wherein the cache memory includes a plurality of levels and is communicatively coupled to a processor unit;

providing an indication to the processor unit, based on the comparing whether the address of the set of data is included in the cache memory, wherein if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included;

establishing a relative amount of time to access the set of data, by the processor unit, based on which level of the plurality of levels the address is included; and

communicating the indication, by the processor unit, to software being executed on the processor unit.

20. (cancelled).

21. (original): A method as described in claim 19, wherein the software is selected from the group consisting of an operating system and an application.

22. (original): A method as described in claim 19, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

23. (original): One or more computer-readable media comprising computer-executable instructions that, when executed, perform the method as recited in claim 19.

Claims 24-41 (cancelled).

42. (previously presented): For use on a processor unit that is communicatively coupled to a comparison unit that is communicatively coupled to a cache memory, a cache residency test instruction, which when executed on the processor unit, configures the comparison unit to perform acts comprising:

comparing an address received from the processor unit with an address in the cache memory;

providing an indication to the processor unit based on the comparing of whether the address is included in the cache memory; and

communicating the indication to an operating system being executed by the processor unit.

43. (original): A cache residency test instruction as described in claim 42, wherein the indication indicates to the processor unit whether the address is included in the cache memory, and if so, at which level of a plurality of levels of the cache memory the address is included.

44. (original): A cache residency test instruction as described in claim 42, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

45. (previously presented): A system comprising:

a cache memory; and

a processor unit communicatively coupled to the cache memory, wherein the processor unit includes a cache residency test instruction that, when executed, configures the processor unit:

to query whether a set of data resides in the cache memory;

to receive an indication from the query of whether the set of data resides in the cache memory;

to establish a relative amount of time to access the set of data; and

to communicate the indication and the relative amount of time to software being executed on the processor unit.

46. (original): A system as described in claim 45, further comprising a comparison unit, wherein execution of the cache residency test instruction by the processor unit configures the comparison unit to compare an address of the set of data with at least one other address of the cache memory in response to the query.

47. (cancelled).

48. (original): A system as described in claim 45, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

49. (original): A system as described in claim 45, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

50. (original): A system as described in claim 45, wherein the cache memory includes a plurality of levels, if the address is included in the cache memory, the indication indicates at which level of the plurality of levels the address is included.

Claims 51-55 (cancelled).

56. (previously presented): A processor chip comprising

a processor unit having a coupling for communicatively coupling the processor unit to a cache memory, wherein:

the processor unit includes storage for a cache residency test instruction; and

an execution of the cache residency test instruction with the processor unit configures the processor unit to determine if a set of data resides in the cache memory, establish a relative amount of time to access the set of data, and communicate a result of the determination and the relative amount of time to software being executed on the processor unit.

57. (original): A processor chip as described in claim 56, further comprising a second processor unit having:

a coupling for communicatively coupled the second processor unit to the cache memory;

storage for a second cache residency test instruction; and

an execution of the second cache residency test instruction with the second processor unit configures the second processor unit to determine if a set of data resides in the cache memory and communicate a result of the determination to software being executed on the second processor unit.

58. (original): A processor chip as described in claim 56, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

59. (original): A processor chip as described in claim 56, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

60. (original): A processor chip as described in claim 56, wherein the cache memory is selected from the group consisting of:

a cache memory located on the processor chip;

a cache memory located off the processor chip; and

a combination of the forgoing.

61. (original): A processor chip as described in claim 56, wherein the cache memory is configured as a semiconductor-based memory.

62. (original): A processor chip as described in claim 56, wherein the software is selected from the group consisting of an operating system and an application.

63. (previously presented): A computing device comprising:

a storage device; and

a processor chip, communicatively coupled to the storage device, and including:

a cache memory; and

a processor unit communicatively coupled to the cache memory, wherein the processor unit includes storage for a cache residency test instruction that, when executed by the processor unit, configures the processor unit to determine if a set of

data resides in the cache memory and to communicate a result of the determination to an operating system being executed on the processor chip.

64. (previously presented): A computing device as described in claim 63, wherein the processor chip further comprises a second processor unit communicatively coupled to the cache memory, wherein the second processor unit includes storage for a second cache residency test instruction that, when executed by the second processor unit, configures the second processor unit to determine if a set of data resides in the cache memory and to communicate a result of the determination to the operating system being executed on the processor chip

65. (original): A computing device as described in claim 63, wherein the set of data is selected from the group consisting of:

an instruction for controlling the processor unit; and

data for being processed by the processor unit.

66. (original): A computing device as described in claim 63, wherein the cache memory is selected from the group consisting of:

a cache memory for storing an instruction for controlling the processor unit;

a cache memory for storing data for being processed by the processor unit; and

a combination of the forgoing.

67. (original): A computing device as described in claim 63, wherein the cache memory is configured as a semiconductor-based memory.

68. (cancelled).

APPENDIX: EVIDENCE

None.

APPENDIX: RELATED PROCEEDINGS

None.